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VLSI VERTICAL CLOCK GENERATING CHIPS FOR THE 160 x 244 AND 320 x 244 PtSi IR CAMERAS

S. DiSalvo and J.E. Murguia

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ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, NY 13441-5700

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APPROVED: Freeman D. Shepherd

FREEMAN D. SHEPHERD
Chief, Electromagnetic Devices Technology Div

APPROVED: Harold Roth

HAROLD ROTH
Director of Solid State Sciences

FOR THE COMMANDER: James W. Hyde III

JAMES W. HYDE III
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DiSalvo, S., Murguia, J.E.

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A VLSI circuit has been designed and fabricated for the RADC platinum silicide infrared camera with the objective being to reduce the size of future cameras by implementing a significant amount of the "front-end" electronics on a single integrated circuit. The "front-end" electronics consists of a clock driver board, a digital timing board, an analog board, a power conditioning board, and a bias control board all located on the sensor head with the IR focal plane and optics. The section of electronics chosen for reduction in this project was the digital timing board responsible for clocking the IR data off the focal plane.

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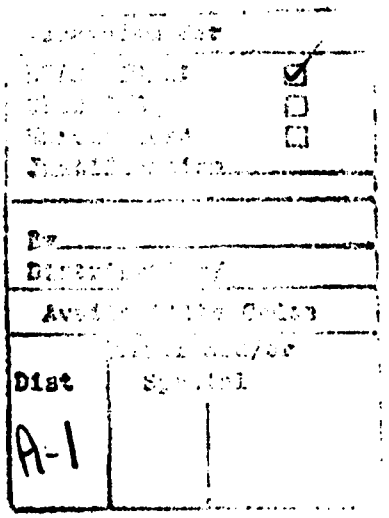


VLSI Vertical Clock Generating Chips for the 160 x 244 and 320 x 244 PtSi IR Cameras

Two custom VLSI clock chips have been designed and fabricated for the RADC platinum silicide infrared cameras. The chips replace several off the shelf IC's on the "front-end" of the camera by producing the CCD vertical clocking required for the 160 x 244 and 320 x 244 PtSi IRCCD focal planes. The technologies used for the project were NMOS and CMOS and the fabrication was done through MOSIS which provides low cost IC fabrication services to government agencies and industry. Each circuit was fabricated using 3 μm technology and packaged on a MOSIS 40 pin chip frame 6.8 mm x 6.9 mm. The NMOS chip included 21,000 transistors while the CMOS version included 1,500 transistors.

The vertical CCD clock circuitry requires a 1.292 MHz input clock to produce 11 unique clock signals each having a period of 33.33 ms, the duration of one frame of data from the IR camera. The NMOS version of this circuit also requires an external reset pulse which can be created by decoding the 16 bit internal counter and feeding it back into the reset input when the cycle has been completed. The CMOS version has automatic reset. The clock signals generated have a total number of 43,050 states in one timing cycle and are made up of four basic time intervals. During the first interval of 158 μs all the clock signals are stopped and the detectors are reset. During the second time interval of 16.5 ms, the circuit produces 130 horizontal blanking pulses enabling the 4-phase CCD pulses to clock the vertical columns of the focal plane. The last two time intervals are repetitions of the first two with the exception of the pulse being used to reset the detectors. Timing diagrams detailing the outputs of the chips are shown in Figures 1, 2, and 3. Outputs are listed in Table 1.

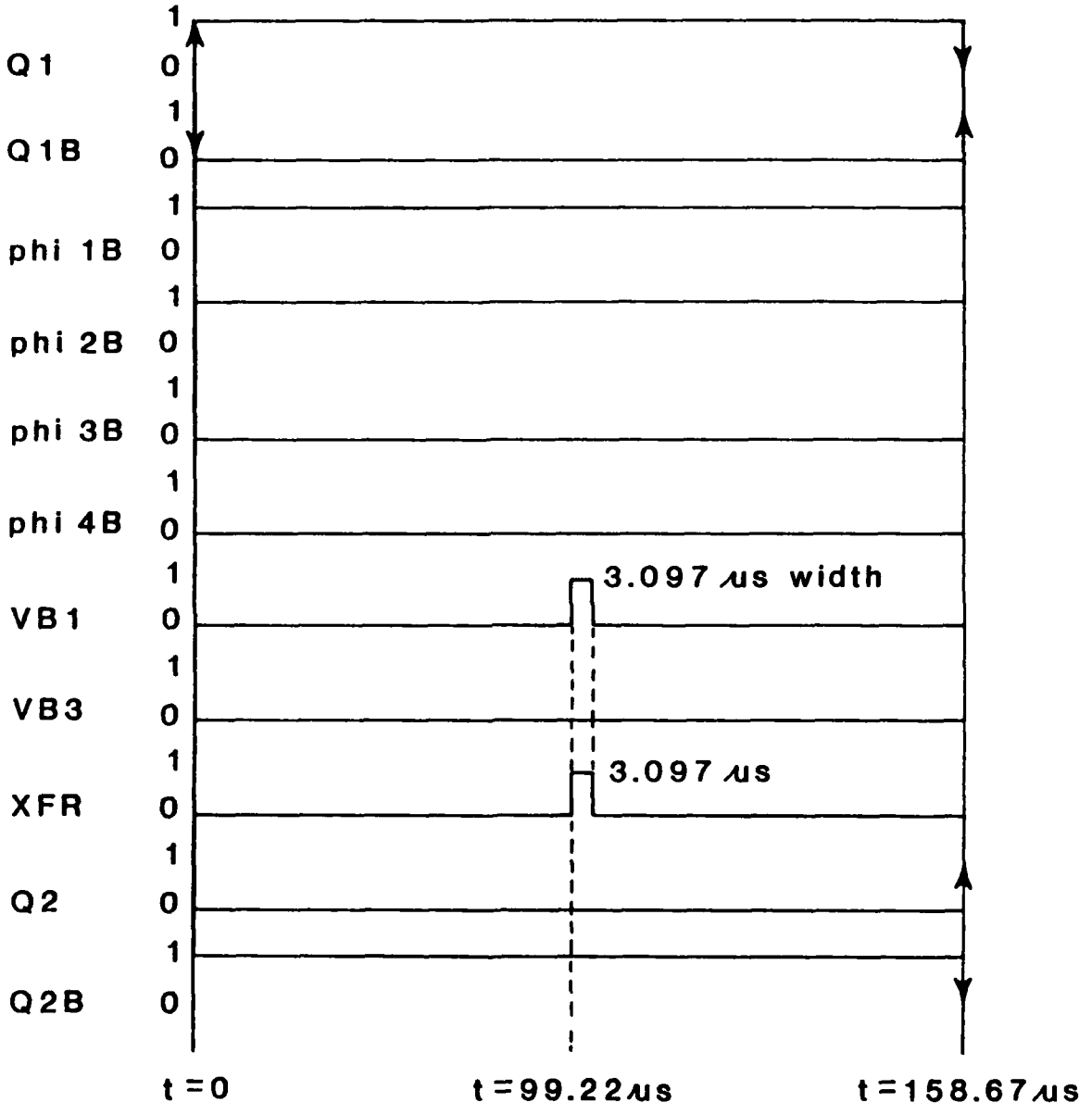
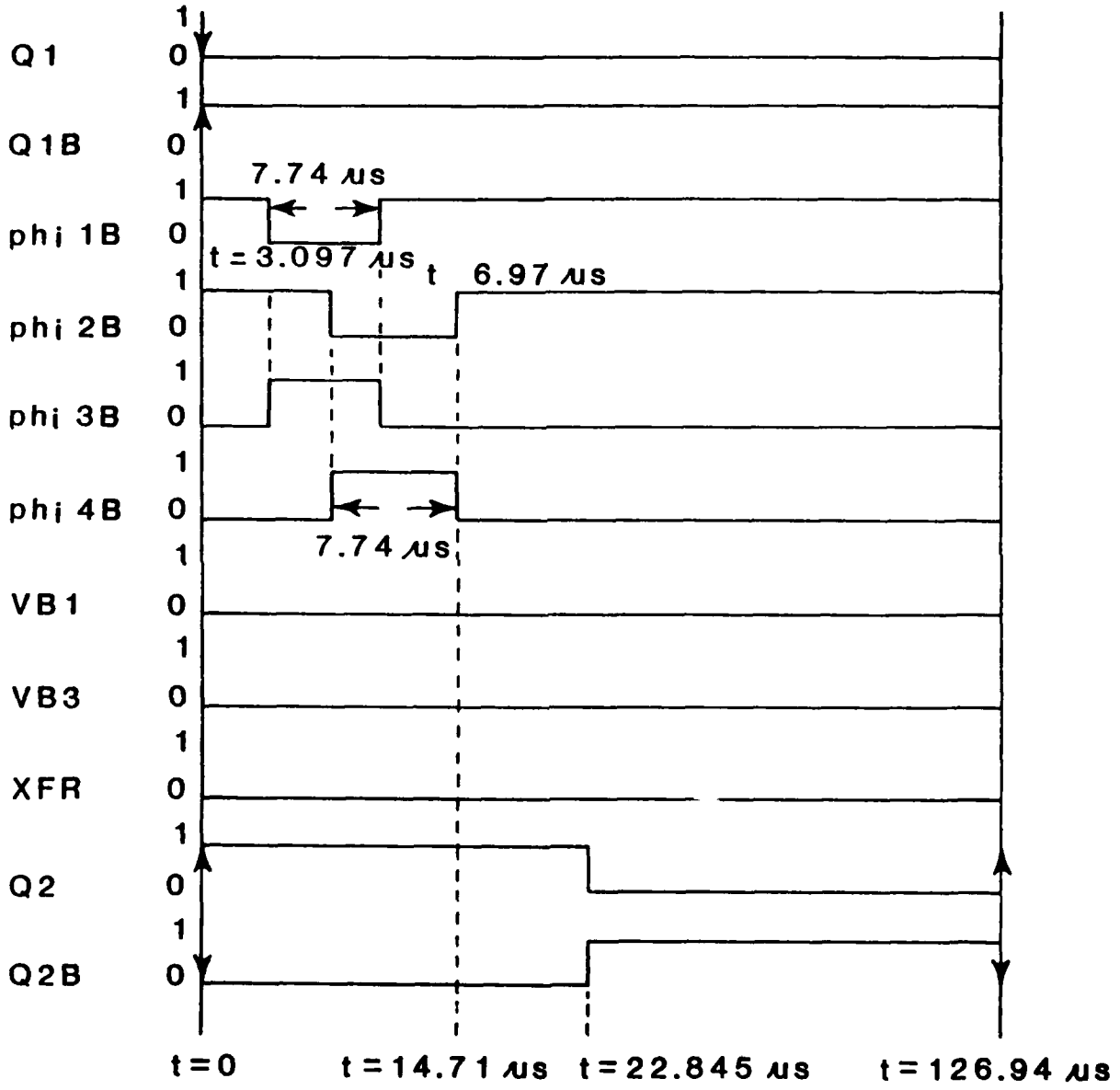


FIGURE 1: TIMING DIAGRAM INTERVAL 1

Figure 1. Timing Diagram Interval 1.



NOTE: This section is repeated 130 times in Interval 2 and 4

Figure 2. Timing Diagram, Intervals 2 and 4.

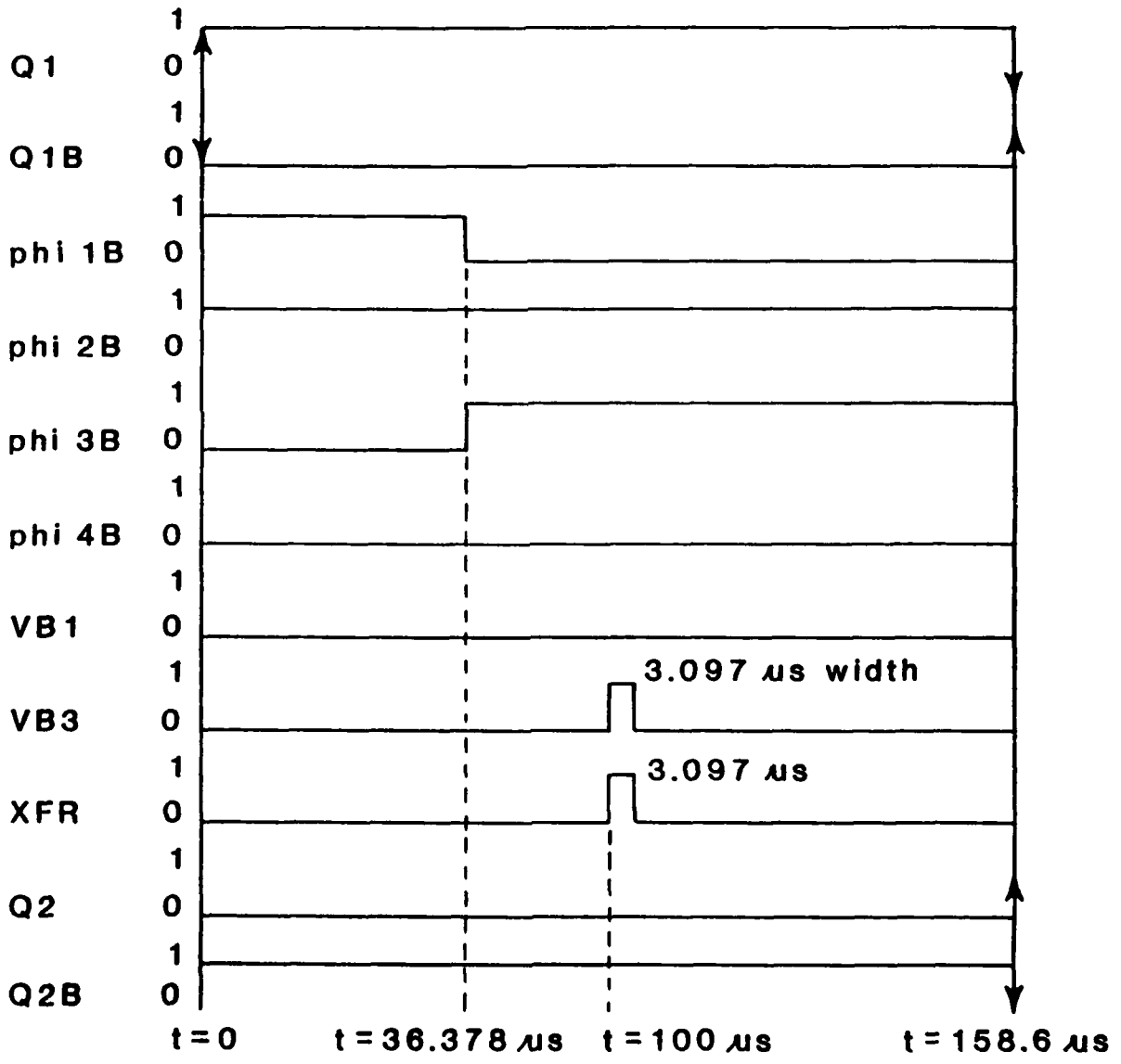


Figure 3. Timing Diagram Interval 3.

Table 1. Outputs Name and Function.

1.	Q-1 - High Equals all Clocks Stopped.
2.	Q1b - High Equals all Clocks Enabled.
3.	VB1 - Detector Reset.
4.	VB3 - Detector Reset.
5.	XFR - Detector Reset Summed.
6.	Q2 - Horizontal Blank (High Equals Vertical Clocking).
7.	Q2b - Horizontal Blank (High Equals Horizontal Clocking).
8.	Phi1b - 4 Phase CCD Clock.
9.	Phi2b - 4 Phase CCD Clock.
10.	Phi3b - 4 Phase CCD Clock.
11.	Phi4b - 4 Phase CCD Clock.

Note: 1C (LSB) through 16C (MSB) are the outputs from the 16 bit counter.

The design of the NMOS clock chip took advantage of the University of California at Berkeley "mpla" program which translates a logic truth table into a Programmable Logic Array. For example, for every state from 0 to 43,049 there exists a corresponding value for each PLA output. States that correspond to low outputs are not required to be entered into the logic truth table. This means that a high output state will correspond to one line in the logic truth table of a PLA. The number of lines in the truth table is directly proportional to the size of the PLA's generated by the mpla program. For the NMOS project, the PLA's were programmed so each time a vertical clock output was required to transition from a low state to a high state, the PLA output would be high. The high output would then set an SR flip-flop and start a counter holding the output high for the desired length of time. A decoder would then generate a reset pulse that would reset the flip-flop at the desired count. This helped eliminate many lines of the truth tables, thus greatly reducing the size of the PLA's. Chip outputs Q2, Q2b, phi1b, phi2b, phi3b, and phi4b were created in this fashion. However, the middle interval of phi1b and phi3b, and outputs Q1, Q1b, VB1, VB3, and XFR were created by including every high state into the logic truth table. This was possible for these outputs because the number of total states involved was only 200 of the possible 43,050 states. A state generator was designed using a ripple binary counter made up of a string of D type flip-flops and full adders. The outputs from the internal 16 bit binary counter are external outputs on both the NMOS and CMOS clock chips. The block diagram detailing the layout of the NMOS clock chip is shown in Figure 4. Pin assignments are listed in Table 2.

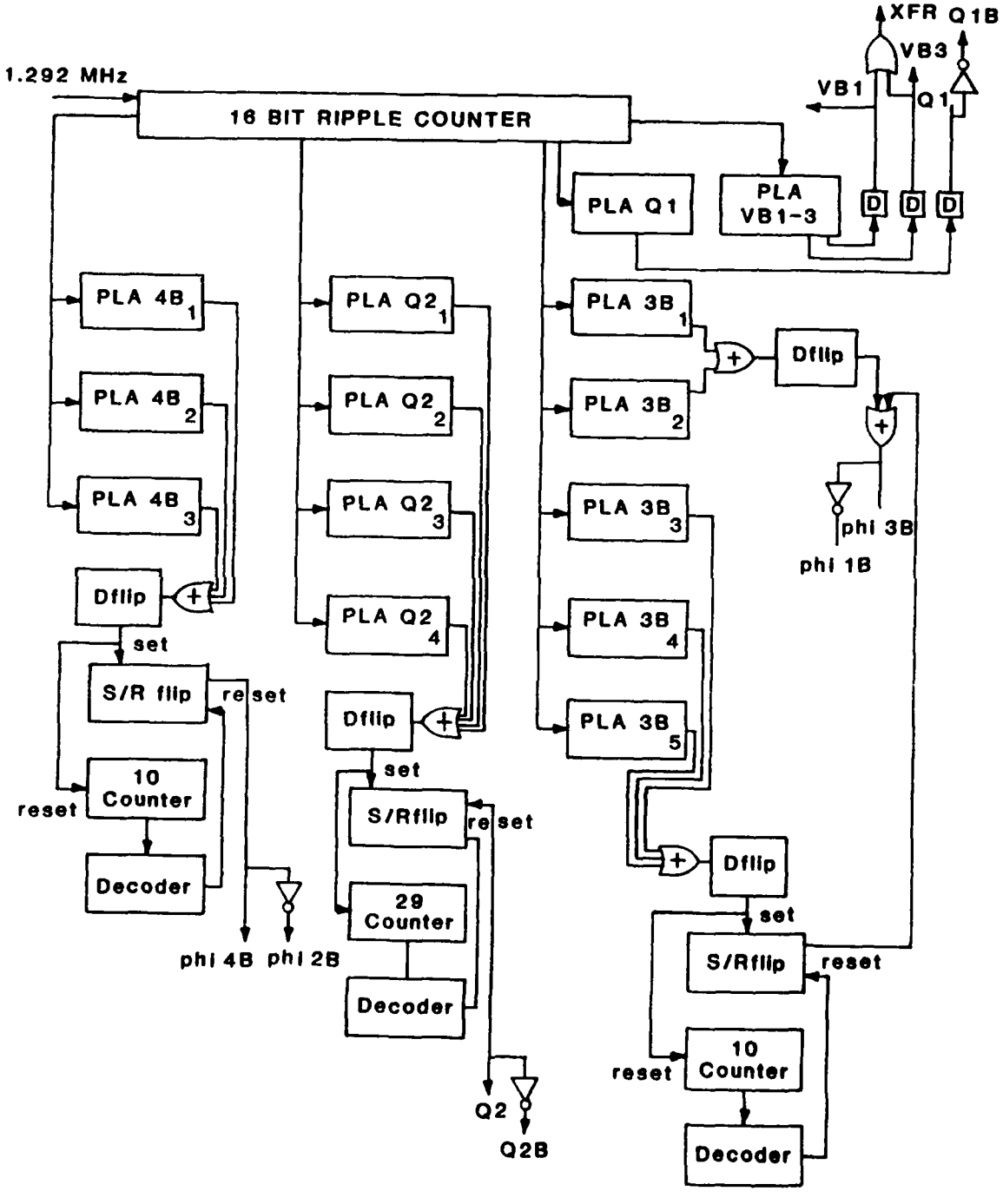


Figure 4. Block Diagram for NMOS Vertical Clock Chip.

Table 2. Pin Assignments for the NMOS Clock Chip.

Pin 1. Phi3b	Pin 21. 11C
Pin 2. Clock/2	Pin 22. 10C
Pin 3. Clock/2 (inverse)	Pin 23. 9C
Pin 4. External Reset (Input)	Pin 24. 8C
Pin 5. Input Clock (1.292 MHz)	Pin 25. 7C
Pin 6. VB1	Pin 26. GND
Pin 7. XFR	Pin 27. Phi2B
Pin 8. VB3	Pin 28. Phi4B
Pin 9. Q1	Pin 29. GND
Pin 10. Q1B	Pin 30. No Connection
Pin 11. 1C	Pin 31. No Connection
Pin 12. 2C	Pin 32. Vdd
Pin 13. 3C	Pin 33. Q2
Pin 14. 4C	Pin 34. Q2B
Pin 15. 5C	Pin 35. 6C
Pin 16. 16C	Pin 36. GND
Pin 17. 15C	Pin 37. Vdd
Pin 18. 14C	Pin 38. GND
Pin 19. 13C	Pin 39. Substrate Connection
Pin 20. 12C	Pin 40. Phi1B

The CMOS clock chip does not include any PLA's and is more compact in design. The state generator is again a 16 bit ripple counter with a 1.292 MHz input clock having a period of 33.33 ms, resulting in 43,050 states. A feedback loop is included enabling the counter to reset once it reaches the final state of the cycle. The block diagram of the CMOS clock chip is shown in Figure 5. Pin assignments are listed in Table 3. Outputs VB1, VB3, Q1, and the intermediate section of phi1b and phi3b are produced via decoding circuitry which decodes the 16 bits from the state generator and sends a set and reset pulse to an SR flip-flop at the proper count. The decoding circuitry which is made up of NAND and NOR gates replaces the bulky PLA structures of the NMOS design. The vertical CCD clocks phi1b through phi4b are controlled by an 8 bit counter which is enabled when Q1 goes low. The 8 bit counter then becomes a "mini state generator" for the 4-phase CCD clocks which are created in similar fashion using decoding circuitry which sends set and reset pulses to SR flip-flops. The mini state generator continues to be reset every 164 input clock pulses which is the period of the 130 horizontal blanking pulses (Q2) that occur between the falling and rising edges of Q1.

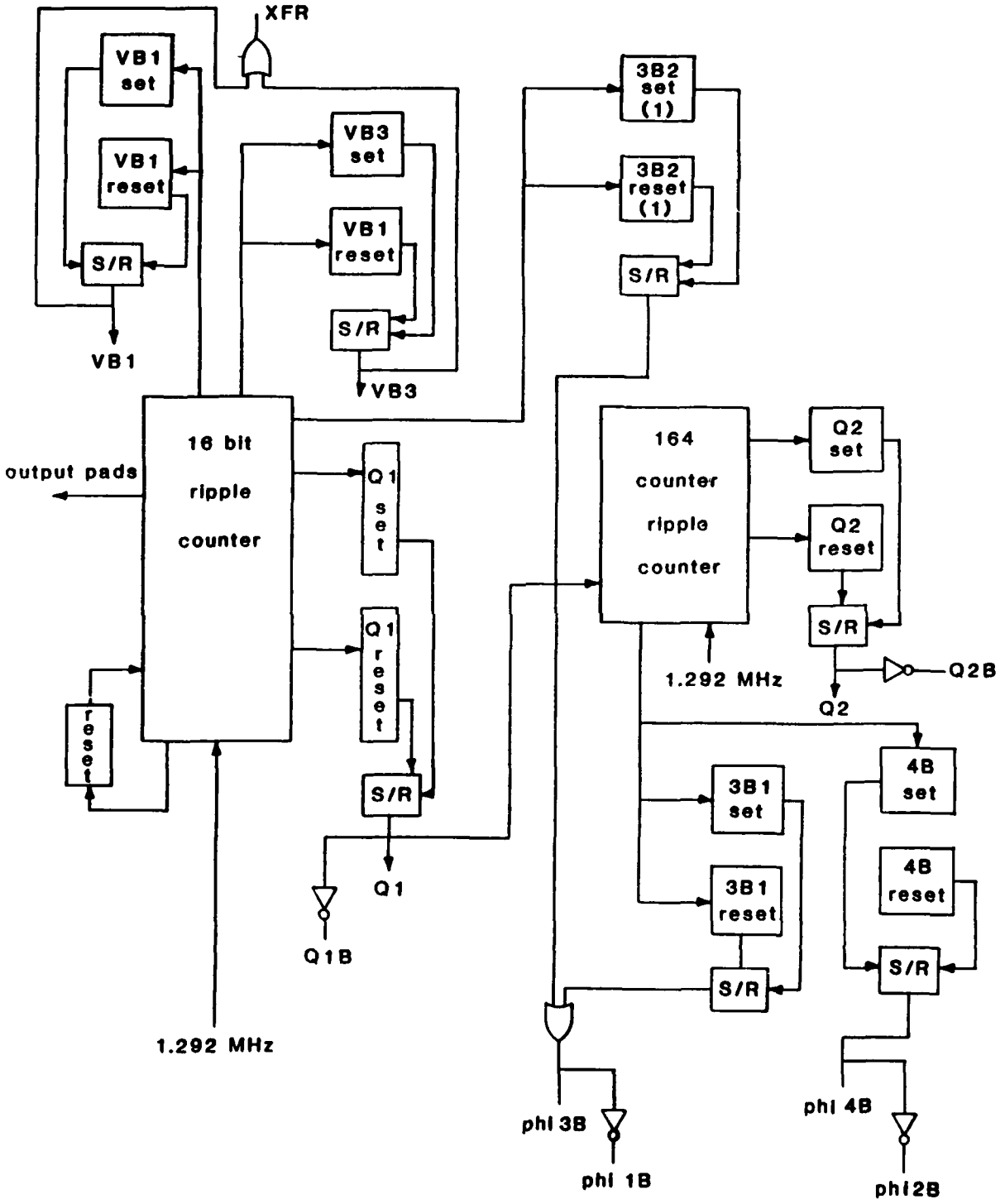


Figure 5. Block Diagram for CMOS Vertical Clock Chip.

Table 3. Pin Assignments for the CMOS Clock Chip.

Pin 1. 3C	Pin 21. Substrate
Pin 2. 4C	Pin 22. Rout (test point)
Pin 3. 5C	Pin 23. Phi2 out (test point)
Pin 4. 6C	Pin 24. No Connection
Pin 5. 7C	Pin 25. No Connection
Pin 6. 8C	Pin 26. Input Clock (1.292 MHz)
Pin 7. 9C	Pin 27. Reset (low)
Pin 8. 10C	Pin 28. No Connection
Pin 9. 11C	Pin 29. GND
Pin 10. 12C	Pin 30. No Connection
Pin 11. 13C	Pin 31. Q1
Pin 12. Vdd	Pin 32. Phi2B
Pin 13. 14C	Pin 33. Phi4B
Pin 14. 15C	Pin 34. Q1B
Pin 15. 16C	Pin 35. Q2
Pin 16. VB3	Pin 36. Q2B
Pin 17. XFR	Pin 37. Phi3B
Pin 18. VB1	Pin 38. Phi1B
Pin 19. No Connection	Pin 39. 1C
Pin 20. No Connection	Pin 40. 2C

Both the NMOS and CMOS chips were designed using Magic, a VLSI layout editor, and simulated extensively with RNL, a logic and timing simulation program. Both software packages were obtained from the University of California at Berkeley. Laboratory testing showed that the NMOS chip could operate up to an input clock speed of 2.0 MHz while the CMOS chip could function properly up to a speed of 2.7 MHz. Future designs have experienced a large increase in speed with more careful consideration given to transistor ratios and routing of signal lines.

The RADC VLSI lab has proven to be a useful tool in designing a custom IC for the PtSi IR camera, however, designs in NMOS with large PLA's are not expected to perform at much higher clock rates than measured for this project. Future CMOS designs fabricated on 2 μm fabrication lines are expected to perform at frequencies beyond 40 MHz.